ISP1110

Universal Serial Bus transceiver with UART signaling

Rev. 02 — 19 March 2007 Product data sheet

1. General description

The ISP1110 is a Universal Serial Bus (USB) transceiver that supports Universal Asynchronous Receiver-Transmitter (UART) signaling mode.

The ISP1110 USB transceiver is fully compliant with *Universal Serial Bus Specification Rev. 2.0*. The ISP1110 can transmit and receive USB data at full-speed (12 Mbit/s).

The ISP1110 transceiver allows USB Application Specific Integrated Circuits (ASICs) with I/O power supply voltage from 1.65 V to 2.85 V to interface to the physical layer of the USB. The transceiver has an integrated 5 V-to-3.3 V voltage regulator for direct powering through USB supply line V_{BUS} and an integrated voltage detector to detect the presence of the V_{BUS} voltage on the $V_{CC(5V0)}$ pin. When V_{BUS} is present, the transceiver is in USB mode. When V_{BUS} is not present, the transceiver can be set to UART signaling mode.

The ISP1110 transceiver is available in HBCC16 lead-free and halogen-free package.

2. Features

- Fully complies with *Universal Serial Bus Specification Rev. 2.0*
- Supports USB data transfer at full-speed (12 Mbit/s)
- Integrated DP pull-up resistor to reduce external components
- Implemented internal DP pull-up resistor as described in *ECN_27%_Resistor*
- Integrated 5 V-to-3.3 V voltage regulator to power through USB line V_{BUS}
- V_{BUS} voltage presence is indicated on pin VBUSDET
- Pins VP and VM function in bidirectional mode, allowing pin count saving for ASIC interface
- Used as a USB peripheral transceiver
- Stable RCV output during Single-Ended Zero (SE0) condition
- Two single-ended receivers with hysteresis
- Low-power operation
- Supports 2.8 V UART signaling mode on the DP and DM lines
- Supports $V_{CC(I/O)}$ voltage range from 1.65 V to 2.85 V
- Supports $V_{CC(UART)}$ voltage range from 2.7 V to 4.5 V
- Off-state supply current from $V_{CC(UART)}$ is less than 3 μA
- Static current from $V_{CC(I/O)}$ is less than 3 μA (typical 1 μA)
- Available in small HBCC16 (3 mm × 3 mm) lead-free and halogen-free package

3. Applications

- Mobile phone
- Personal Digital Assistant (PDA)
- Other portable devices

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
ISP1110VH	HBCC16	plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 × 3 × 0.65 mm	SOT639-2

5. Block diagram

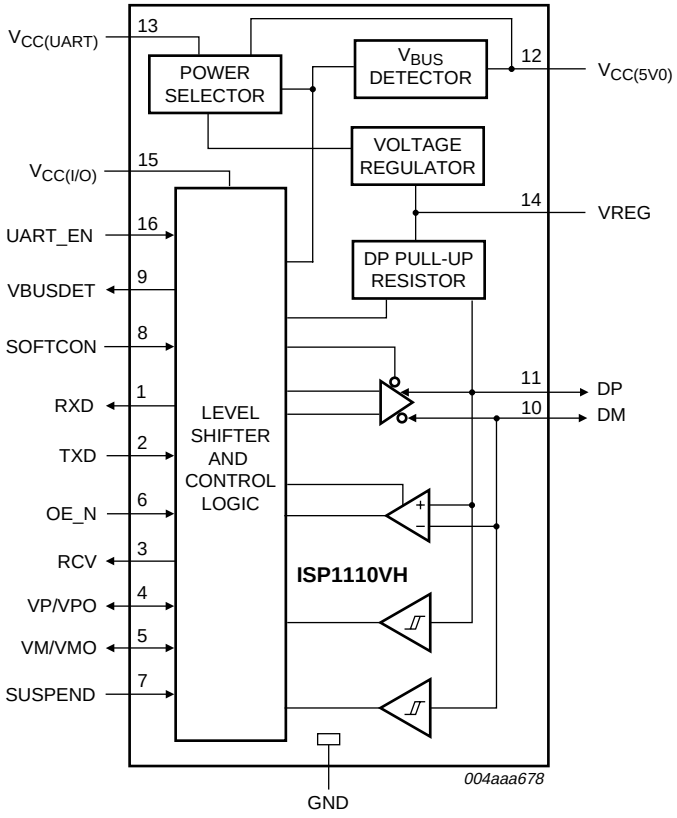
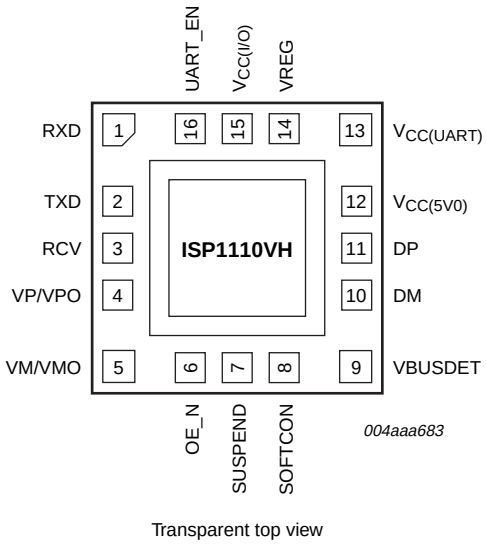


Fig 1. Block diagram

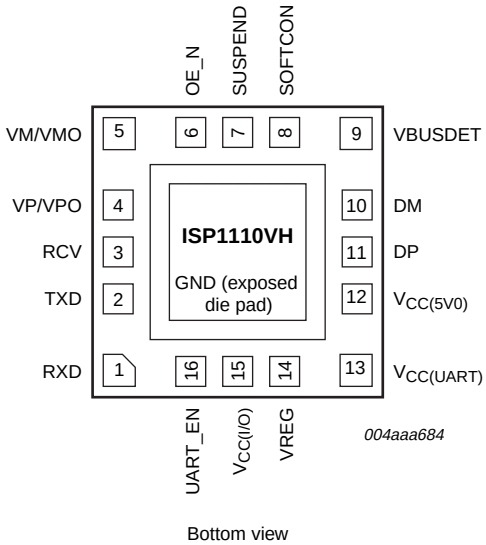
6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration HBCC16; top view



Bottom view

Fig 3. Pin configuration HBCC16; bottom view

6.2 Pin description

Table 2. Pin description

Symbol[1]	Pin	Type[2]	Description
RXD	1	O	UART RXD output to microcontroller (CMOS level with respect to $V_{CC(I/O)}$); driven LOW in USB mode output pad; push pull; 4 mA output drive; CMOS
TXD	2	I	UART TXD input from microcontroller (CMOS level with respect to $V_{CC(I/O)}$) input pad; push pull; CMOS
RCV	3	O	differential data receiver output (CMOS level with respect to $V_{CC(I/O)}$); driven LOW when input SUSPEND is HIGH; the output state of RCV is preserved and stable during an SE0 condition; driven LOW when in UART mode output pad; push pull; 4 mA output drive; CMOS
VP/VPO	4	I/O	single-ended DP receiver output VP (CMOS level with respect to $V_{CC(I/O)}$); for external detection of SE0, error conditions and speed of connected device; this pin also acts as drive data input VPO; see Table 5 and Table 6 bidirectional pad; push-pull input; 3-state output; 4 mA output drive; CMOS
VM/VMO	5	I/O	single-ended DM receiver output VM (CMOS level with respect to $V_{CC(I/O)}$); for external detection of SE0, error conditions and speed of connected device; this pin also acts as drive data input VMO; see Table 5 and Table 6 bidirectional pad; push-pull input; 3-state output; 4 mA output drive; CMOS
OE_N	6	I	USB output enable (CMOS level with respect to $V_{CC(I/O)}$, active LOW); enables the transceiver to transmit data on the USB bus input pad; push pull; CMOS
SUSPEND	7	I	suspend input (CMOS level with respect to $V_{CC(I/O)}$); a HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a LOW level; this pin is ignored when in UART mode input pad; push pull; CMOS
SOFTCON	8	I	software controlled USB connection input; a HIGH level enables the internal DP pull-up resistor when VBUSDET is HIGH; this pin is ignored when in UART mode input pad; push pull; CMOS
VBUSDET	9	O	V_{BUS} indicator output (CMOS level with respect to $V_{CC(I/O)}$); when $V_{BUS} > V_{CC(5V0)th}$, then VBUSDET = HIGH and when $V_{BUS} < V_{CC(5V0)th}$, then VBUSDET = LOW output pad; push pull; 4 mA output drive; CMOS
DM	10	AI/O	**USB mode —** Negative USB data bus connection (analog, bidirectional, differential) **UART mode —** UART TXD line (digital output)
DP	11	AI/O	**USB mode —** Positive USB data bus connection (analog, bidirectional, differential) **UART mode —** UART RXD line (digital input)

Table 2. Pin description *...continued*

Symbol[1]	Pin	Type[2]	Description
$V_{CC(5V0)}$	12	-	supply voltage input (4.0 V to 5.5 V); can be directly connected to USB line V_{BUS}
$V_{CC(UART)}$	13	-	supply voltage input (2.7 V to 4.5 V) for the UART signaling
VREG	14	-	internal regulator output; a decoupling capacitor of at least 0.1 µF is required
$V_{CC(I/O)}$	15	-	supply voltage for digital I/O pins (1.65 V to 2.85 V). When $V_{CC(I/O)}$ is not connected, the DP and DM pins are in off-state. This supply pin is totally independent of $V_{CC(5V0)}$ and VREG, and must never exceed VREG.
UART_EN	16	I	enable UART signaling mode when $V_{CC(5V0)}$ is not present input pad; push-pull; CMOS
GND	exposed die pad	-	ground supply; down bonded to the exposed die pad (heat sink); to be connected to the PCB ground

[1] Symbol names ending with underscore N, for example, _N, indicate active LOW signals.

[2] I = input; O = output; I/O = digital input/output; AI/O = analog input/output.

7. Functional description

7.1 Modes of operation

The ISP1110 supports two modes of operation:

- USB mode (3.3 V signaling)
- UART mode (2.8 V signaling)

Table 3 shows the definition of various operating modes.

Table 3. Operating modes: definition

$V_{CC(I/O)}$	$V_{CC(UART)}$	$V_{CC(5V0)} = V_{BUS}$	UART_EN	Mode
Off	X	X	X	not defined
On	X	off	LOW	isolate mode
On	on	off	HIGH	UART mode
On	X	on	LOW	USB mode

Table 4 shows the pin status in various operating modes.

Table 4. Pin status in various modes

Pin	Isolate mode	UART mode	USB mode
DP	not powered	high-Z	see Table 5
DM	not powered	driven (= TXD)	see Table 5
VP/VPO, VM/VMO	high-Z	LOW when OE_N = HIGH	see Table 5
		high-Z when OE_N = LOW	
RCV	LOW	LOW	see Table 5
VBUSDET	LOW	LOW	HIGH
RXD	LOW	driven (= DP)	LOW
UART_EN, TXD, SUSPEND, SOFTCON, OE_N	high-Z	high-Z	high-Z
VREG	not powered	2.8 V	3.3 V

7.1.1 USB mode

When the ISP1110 is in USB mode, pins DP and DM work as the USB D+ and D– lines, respectively. The DP and DM driver is powered by VREG. The USB function is compatible with the ISP1102 transceiver.

When the ISP1110 is in USB mode, the TXD input pin is ignored and the RXD output pin is driven LOW.

The ISP1110 is in USB mode when $V_{CC(5V0)} > V_{CC(5V0)th}$ and UART_EN is LOW. $V_{CC(I/O)}$ must be on.

A short description of the USB detection sequence is:

1. The phone is connected to the USB port of a powered PC.
2. The ISP1110 detects V_{BUS} is above $V_{CC(5V0)th}$. The ISP1110 enters USB mode and the Analog USB Transceiver (ATX) is powered by VREG.

3. If the phone is switched off ($V_{CC(I/O)}$ is not present), then the DP and DM pins of the ISP1110 remain at high-impedance and the PC will not detect any device attachment.
4. If the phone is switched on ($V_{CC(I/O)}$ is present), then the ISP1110 will drive the VBUSDET pin to a HIGH level.
5. The phone processor detects that pin VBUSDET is HIGH. If the phone system software is ready for USB operation, the phone processor will assert pin SOFTCON.
6. The ISP1110 will enable the DP pull-up resistor ($R_{PU(DP)}$).
7. The PC detects DP at the HIGH level and starts the USB full-speed enumeration.
8. The PC loads the driver for the phone, if enumeration is successful.

For the flowchart, see Section 7.1.3.

7.1.2 UART mode

When the ISP1110 is in UART mode, the DP and DM driver is powered by 2.8 V. The ISP1110 works as a level shifter between these pairs of pins:

- From TXD ($V_{CC(I/O)}$ level) to DM (2.8 V level).
- From DP (2.8 V level) to RXD ($V_{CC(I/O)}$ level).

When the ISP1110 is in UART mode, the USB differential receiver is disabled. The SUSPEND and SOFTCON input pins are ignored. The RCV pin is driven LOW. The VP/VPO and VM/VMO pins are driven LOW, if OE_N is HIGH. The VP/VPO and VM/VMO pins are 3-state LOW, if OE_N is LOW.

The ISP1110 is in UART mode when $V_{CC(5V0)} < V_{CC(5V0)th}$ and pin UART_EN is HIGH. $V_{CC(I/O)}$ and $V_{CC(UART)}$ must be on.

A short description of the UART detection sequence is:

1. The phone is switched on ($V_{CC(I/O)}$ is present).
2. If V_{BUS} is off, the ISP1110 will drive VBUSDET to a LOW level. The ATX is powered by 2.8 V.
3. The ISP1110 will enter UART signaling mode, if UART_EN is HIGH.

For the flowchart, see Section 7.1.3.

7.1.3 Mode detection flowchart

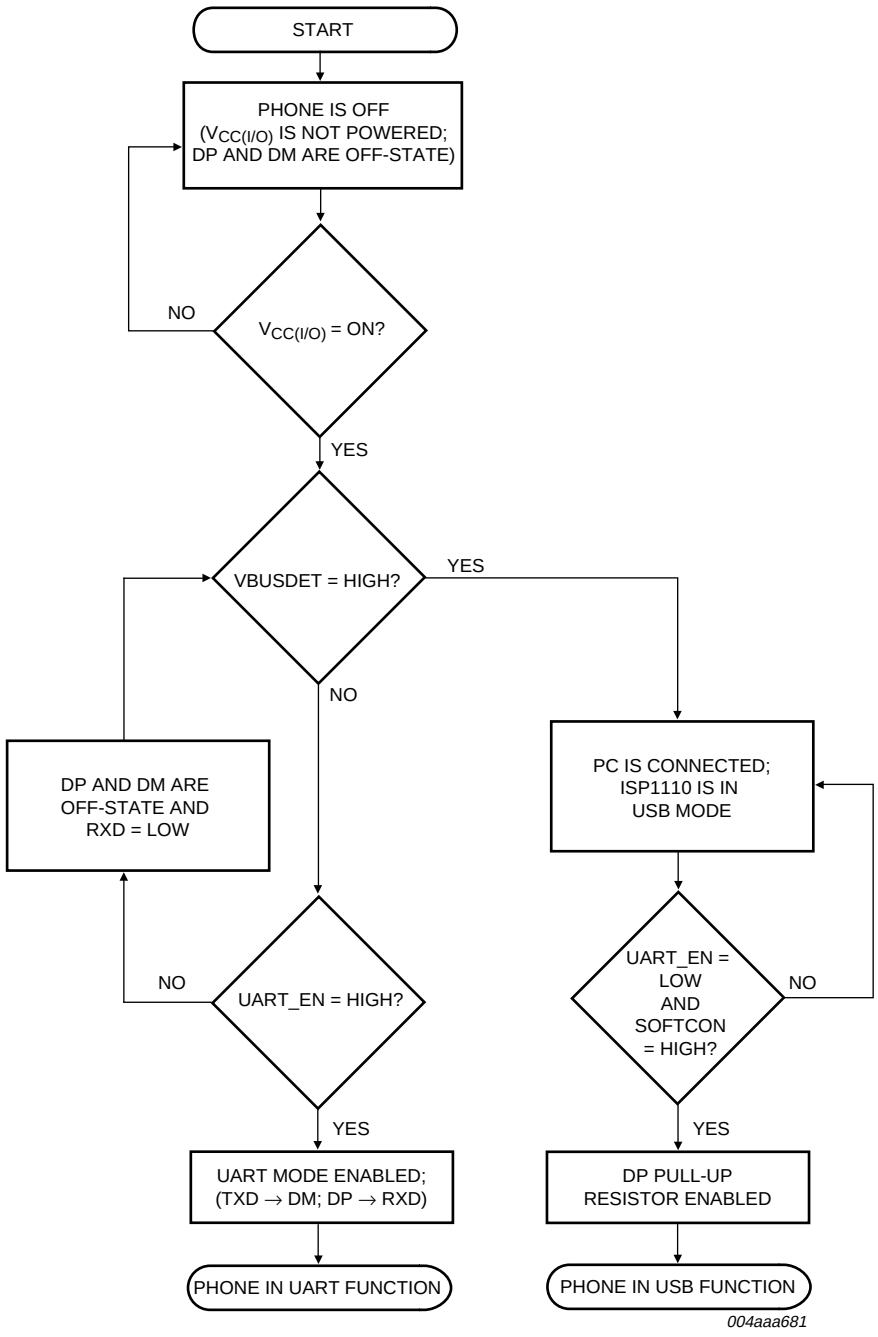


Fig 4. ISP1110 mode detection flowchart

7.1.4 Mode switching time

When the USB cable is connected, the ISP1110 is in USB mode. When the USB cable is removed and the UART cable is connected, the ISP1110 may switch to UART mode as long as the VBUSDET output is LOW. On the other hand, if the UART cable is removed and the USB cable is connected, the ISP1110 can switch to USB mode.

UART mode cannot be enabled until the voltage on $V_{CC(5V0)}$ drops below the VBUSDET threshold (0.8 V to 4.0 V). Therefore, the time required to switch from USB mode to UART mode is determined by the RC discharge time on the V_{BUS} line. Given that $V_{CC(5V0)}$ = 5.0 V, R = 100 kΩ and C = 1 μF, the discharge time is less than 200 ms (from 5 V to 0.8 V). Assume the detection of the UART cable connect or disconnect is very fast (within 1 ms), the total switching time from the USB cable removal to entering UART mode can be less than 200 ms. The total switching time from the UART cable removal to entering USB mode can be less than 200 ms.

When VBUSDET becomes LOW, it is recommended that you wait for 50 ms before asserting UART_EN. This is because there is no hysteresis built for the VBUSDET threshold detector.

The time between VBUSDET going HIGH and SOFTCON assertion is 0 ms to 100 ms, according to *Universal Serial Bus Specification Rev. 2.0, Section 7.1.7.3*.

7.2 Analog USB Transceiver (ATX)

The ISP1110 ATX supports USB full-speed (12 Mbit/s) signaling. The ATX function is compatible with the ISP1102 transceiver. Table 5 shows the function of the ATX.

Table 5. USB function

SUSPEND	OE_N	DP and DM	RCV	VP/VPO	VM/VMO	Function
LOW	LOW	driving/receiving	active	VPO input	VMO input	normal driving (differential receiver active)
LOW	HIGH	receiving[1]	active	VP output	VM output	receiving
HIGH	LOW	driving	inactive[2]	VPO input	VMO input	driving during suspend (differential receiver inactive)
HIGH	HIGH	high-Z[1]	inactive[2]	VP output	VM output	low-power state

[1] Signal levels on the DP and DM pins are determined by other USB devices and external pull-up or pull-down resistors.

[2] In suspend mode (SUSPEND = HIGH), the differential receiver is inactive and output RCV is always LOW. The resume signaling is detected through single-ended receivers VP/VPO and VM/VMO.

Table 6. USB driving function (pin OE_N = LOW)

VM/VMO	VP/VPO	Data
LOW	LOW	SE0
LOW	HIGH	differential logic 1
HIGH	LOW	differential logic 0
HIGH	HIGH	illegal state

Table 7. USB receiving function (pin OE_N = HIGH)

DP, DM	RCV	VP/VPO	VM/VMO
Differential logic 0	LOW	LOW	HIGH
Differential logic 1	HIGH	HIGH	LOW
SE0	RCV*[1]	LOW	LOW

[1] RCV* denotes the signal level on output RCV just before the SE0 state occurs. This level is stable during the SE0 period.

7.3 V_{BUS} detector

The V_{BUS} detector provides voltage level detection on V_{BUS}, if V_{BUS} is connected to $V_{CC(5V0)}$. If V_{BUS} is greater than V_{BUS} valid threshold $V_{CC(5V0)th}$, pin VBUSDET will output a HIGH level. Otherwise, pin VBUSDET will output a LOW level.

The V_{BUS} detector is powered by $V_{CC(I/O)}$.

7.4 DP pull-up resistor

The internal DP pull-up resistor is connected between the VREG and DP pins, if pin SOFTCON is a HIGH level.

The pull-up resistor is context variable, as described in document *ECN_27%_Resistor*. The variable pull-up resistor hardware is implemented here to meet the *ECN_27%_Resistor* specification.

7.5 DC-DC regulator

In USB mode, when $V_{CC(5V0)}$ = 4.0 V to 5.5 V, the regulator will output 3.0 V to 3.6 V. In UART mode, when $V_{CC(UART)}$ = 2.7 V to 4.5 V, the regulator will output 2.35 V to 2.85 V.

A 0.1 μF capacitor is required to connect to the VREG pin.

7.6 Power selector

When VBUSDET = HIGH, the regulator will be powered by $V_{CC(5V0)}$. When VBUSDET = LOW and UART_EN = HIGH, the regulator will be powered by $V_{CC(UART)}$.

When $V_{CC(I/O)}$ is not connected, the DP and DM output will be in off-state.

For proper operation, the $V_{CC(I/O)}$ voltage must not exceed VREG.

8. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)			–0.5	+6.0	V
$V_{CC(UART)}$	supply voltage (UART)			–0.5	+5.5	V
$V_{CC(I/O)}$	input/output supply voltage			–0.5	+4.6	V
V_I	input voltage			–0.5	$V_{CC(I/O)}$ + 0.5 V	V
I_{lu}	latch-up current	V_I = –1.8 V to +5.4 V		-	100	mA
V_{ESD}	electrostatic discharge voltage	all pins; I_{LI} < 1 µA	[1]	–2000	+2000	V
		pins DP, DM, $V_{CC(5V0)}$, GND; I_{LI} < 3 µA; 1 µF capacitor on $V_{CC(5V0)}$	[1]	–3000	+3000	V
T_{stg}	storage temperature			–40	+125	°C

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor (Human Body Model).

9. Recommended operating conditions

Table 9. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)		4.0	5.0	5.5	V
$V_{CC(UART)}$	supply voltage (UART)		2.7	-	4.5	V
$V_{CC(I/O)}$	input/output supply voltage		1.65	1.8	2.85	V
V_I	input voltage		0	-	$V_{CC(I/O)}$	V
$V_{IA(I/O)}$	input voltage on analog I/O pins	pins DP and DM	0	-	3.6	V
T_{amb}	ambient temperature		–40	-	+85	°C
T_j	junction temperature		–40	-	+125	°C

10. Static characteristics

Table 10. Static characteristics: supply pins

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = –40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{O(VREG)}$	output voltage on pin VREG	USB mode	[1]	3.0	3.3	3.6	V
		UART mode		2.35	2.6	2.85	V
$I_{CC(5V0)}$	supply current (5.0 V)	USB mode; transmitting and receiving at 12 Mbit/s; C_L = 50 pF on pins DP and DM	[2]	-	4	8	mA
$I_{CC(UART)}$	supply current (UART)	UART mode; 921.6 kbit/s		-	-	4	mA
$I_{CC(I/O)}$	supply current on pin $V_{CC(I/O)}$	transmitting and receiving at 12 Mbit/s	[2]	-	1	2	mA

Table 10. Static characteristics: supply pins *…continued*

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{CC(5V0)(idle)}$	idle and SE0 supply current (5.0 V)	USB mode; idle: V_{DP} > 2.7 V, V_{DM} < 0.3 V; SE0: V_{DP} < 0.3 V, V_{DM} < 0.3 V	[3]	-	-	300	µA
$I_{CC(I/O)(static)}$	static supply current on pin $V_{CC(I/O)}$			-	-	3	µA
$I_{CC(5V0)(susp)}$	suspend mode supply current (5.0 V)	USB mode SUSPEND = HIGH	[3]	-	-	35	µA
$I_{CC(UART)(off)}$	off-state supply current (UART)	USB mode or UART_EN = LOW		-	-	3	µA
$V_{CC(5V0)th}$	supply voltage detection threshold (5.0 V)	1.65 V ≤ $V_{CC(I/O)}$ ≤ 2.85 V		0.8	-	4.0	V
$V_{CC(I/O)th}$	supply voltage detection threshold (I/O)			0.5	-	1.4	V

[1] The minimum voltage is 2.7 V in suspend mode.

[2] Maximum value characterized only, not tested in production.

[3] Excluding any load current and source current to the DP/DM pull-up and pull-down resistors (200 µA typical).

Table 11. Static characteristics: digital pins

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{CC(I/O)}$ = 1.65 V to 2.85 V							
Input levels							
V_{IL}	LOW-level input voltage			-	-	$0.3V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{CC(I/O)}$	-	-	V
Output levels							
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA		-	-	0.15	V
		I_{OL} = 2 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA		$V_{CC(I/O)}$ − 0.15 V	-	-	V
		I_{OH} = 2 mA		$V_{CC(I/O)}$ − 0.4 V	-	-	V
Leakage current							
I_{LI}	input leakage current		[1]	−1	-	+1	µA
Capacitance							
C_{in}	input capacitance	pin to GND		-	-	10	pF
Example 1: $V_{CC(I/O)}$ = 1.8 V ± 0.15 V							
Input levels							
V_{IL}	LOW-level input voltage			-	-	0.5	V
V_{IH}	HIGH-level input voltage			1.2	-	-	V
Output levels							
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA		-	-	0.15	V
		I_{OL} = 2 mA		-	-	0.4	V

Table 11. Static characteristics: digital pins *...continued*

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	1.5	-	-	V
		I_{OH} = 2 mA	1.25	-	-	V
Example 2: $V_{CC(I/O)}$ = 2.775 V ± 0.075 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		3.0	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	2.55	-	-	V
		I_{OH} = 2 mA	2.3	-	-	V

[1] If $V_{CC(I/O)} \geq V_{CC(UART)}$, then the leakage current will be higher than the specified value when in UART mode.

Table 12. Static characteristics: analog I/O pins DP and DM

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input levels (USB mode)							
Differential receiver							
V_{DI}	differential input sensitivity	$\|V_{DP} - V_{DM}\|$		0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range		0.8	-	2.5	V
Single-ended receiver							
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{hys}	hysteresis voltage			0.4	-	0.7	V
Input levels (UART mode)							
V_{IL}	LOW-level input voltage			−0.3	-	+0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	3.0	V
V_{hys}	hysteresis voltage			0.4	-	0.7	V
Output levels (USB mode)							
V_{OL}	LOW-level output voltage	R_L = 1.5 kΩ to 3.6 V		-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L = 15 kΩ to GND	[1]	2.8	-	3.6	V
Output levels (UART mode)							
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		−0.1	-	+0.37	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		2.16	-	2.85	V
Leakage current							
I_{LZ}	off-state leakage current			−1	-	+1	µA
Capacitance							
C_{in}	input capacitance	pin to GND		-	-	10	pF

Table 12. Static characteristics: analog I/O pins DP and DM *…continued*

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Resistance							
Z_{DRV}	driver output impedance	steady-state drive	[2]	34	39	44	Ω
Z_{INP}	input impedance			10	-	-	MΩ
$R_{PU(DP)}$	pull-up resistance on pin DP	bus idle		900	-	1575	Ω
		bus active		1425	-	3090	Ω
Termination							
V_{TERM}	termination voltage	for upstream port pull-up ($R_{PU(DP)}$)	[3][4]	3.0	-	3.6	V

[1] $V_{OH(min)}$ = VREG − 0.2 V.

[2] Includes external resistors of 33 Ω ± 1 % on pins DP and DM.

[3] This voltage is available at pin VREG.

[4] The minimum voltage is 2.7 V in suspend mode.

11. Dynamic characteristics

Table 13. Dynamic characteristics: analog I/O pins DP and DM

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Driver characteristics (UART mode)							
t_{LR}	transition time: rise time	C_L < 250 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$; see Figure 5	[1]	50	-	200	ns
t_{LF}	transition time: fall time	C_L < 250 pF; 90 % to 10 % of $\|V_{OH} - V_{OL}\|$; see Figure 5	[1]	50	-	200	ns
Driver characteristics (USB mode)							
t_{FR}	rise time	C_L = 50 pF to 125 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$; see Figure 5		4	-	20	ns
t_{FF}	fall time	C_L = 50 pF to 125 pF; 90 % to 10 % of $\|V_{OH} - V_{OL}\|$; see Figure 5		4	-	20	ns
FRFM	differential rise time/fall time matching	excluding the first transition from Idle state	[2]	90	-	111.1	%
V_{CRS}	output signal crossover voltage	excluding the first transition from Idle state; see Figure 6	[3]	1.3	-	2.0	V
Driver timing							
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	VPO, VMO to DP, DM; see Figure 6 and Figure 9		-	-	18	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	VPO, VMO to DP, DM; see Figure 6 and Figure 9		-	-	18	ns
t_{PHZ}	driver disable delay from HIGH level	OE_N to DP, DM; see Figure 7 and Figure 10		-	-	15	ns
t_{PLZ}	driver disable delay from LOW level	OE_N to DP, DM; see Figure 7 and Figure 10		-	-	15	ns

Table 13. Dynamic characteristics: analog I/O pins DP and DM *...continued*

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PZH}	driver enable delay to HIGH level	OE_N to DP, DM; see Figure 7 and Figure 10	-	-	15	ns
t_{PZL}	driver enable delay to LOW level	OE_N to DP, DM; see Figure 7 and Figure 10	-	-	15	ns
Receiver timings						
Differential receiver						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP, DM to RCV; see Figure 8 and Figure 11	-	-	15	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP, DM to RCV; see Figure 8 and Figure 11	-	-	15	ns
Single-ended receiver						
$t_{PLH(se)}$	single-ended propagation delay (LOW to HIGH)	DP, DM to VP/VPO, VM/VMO; see Figure 8 and Figure 11	-	-	18	ns
$t_{PHL(se)}$	single-ended propagation delay (HIGH to LOW)	DP, DM to VP/VPO, VM/VMO; see Figure 8 and Figure 11	-	-	18	ns

[1] For UART TXD on pin DM.

[2] t_{FR} / t_{FF}.

[3] Characterized only, not tested. Limits guaranteed by design.

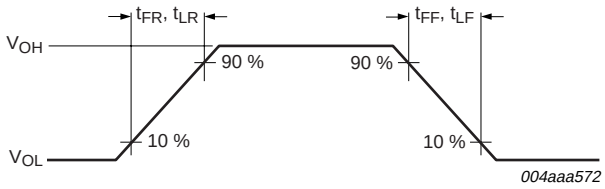


Fig 5. Rise time and fall time

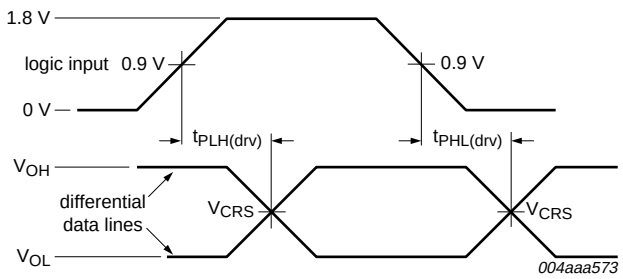


Fig 6. Timing of VPO and VMO to DP and DM

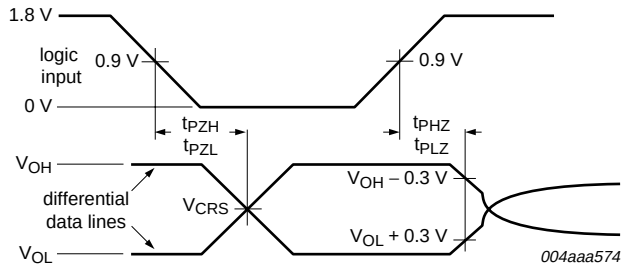


Fig 7. Timing of OE_N to DP and DM

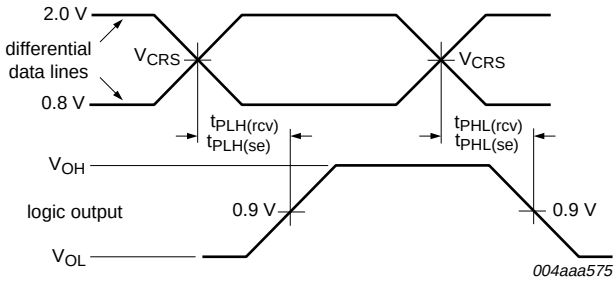
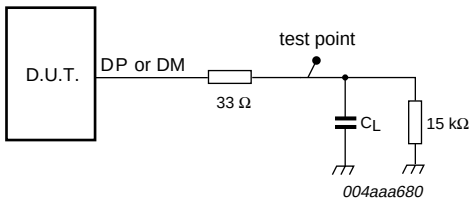


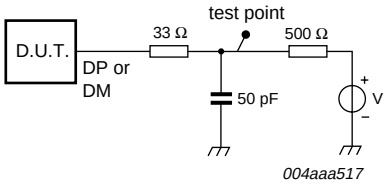
Fig 8. Timing of DP and DM to RCV, VP/VPO and VM/VMO

12. Test information



Load capacitance C_L = 50 pF (minimum or maximum timing)

Fig 9. Load on pins DP and DM



V = 0 V for t_{PZH} and t_{PHZ}

V = VREG for t_{PZL} and t_{PLZ}

Fig 10. Load on pins DP and DM for enable time and disable time

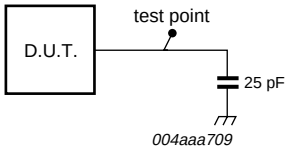
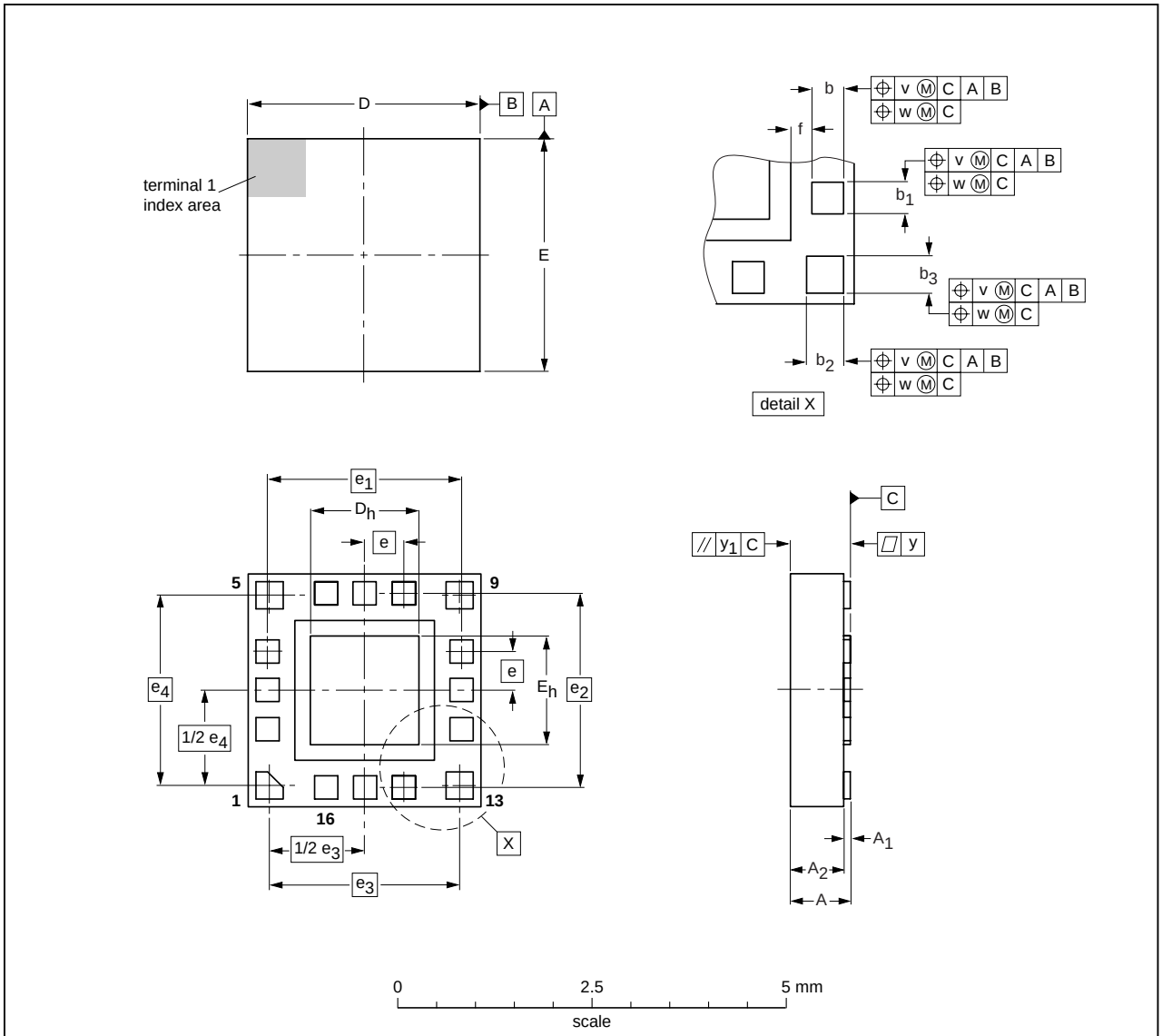


Fig 11. Load on pins VM/VMO, VP/VPO and RCV

13. Package outline

HBCC16: plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 x 3 x 0.65 mm **SOT639-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	b_1	b_2	b_3	D	D_h	E	E_h	e	e_1	e_2	e_3	e_4	f	v	w	y	y_1
mm	0.8	0.10 0.05	0.7 0.6	0.33 0.27	0.33 0.27	0.38 0.32	0.38 0.32	3.1 2.9	1.45 1.35	3.1 2.9	1.45 1.35	0.5	2.5	2.5	2.45	2.45	0.23 0.17	0.08	0.1	0.05	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT639-2		MO-217				01-11-13 03-03-12

Fig 12. Package outline SOT639-2 (HBCC16)

14. Packing information

The ISP1110VH (HBCC16 package) is delivered on a Type A carrier tape, see Figure 13. The tape dimensions are given in Table 14.

The reel diameter is 330 mm. The reel is made of polystyrene and is not designed for use in a baking process.

The cumulative tolerance of 10 successive sprocket holes is ±0.02 mm. The camber must not exceed 1 mm in 100 mm.

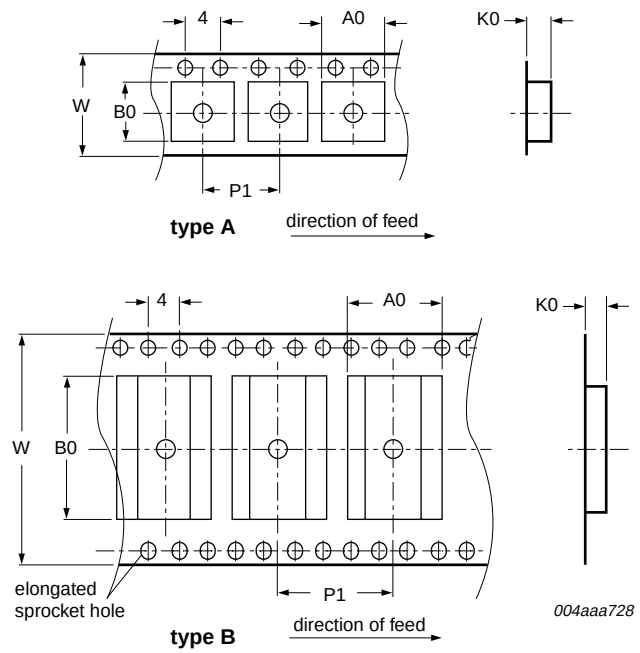


Fig 13. Carrier tape dimensions

Table 14. Type A carrier tape dimensions for the ISP1110VH

Dimension	Value	Unit
A0	3.3	mm
B0	3.3	mm
K0	1.1	mm
P1	8.0	mm
W	12.0 ± 0.3	mm

15. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 14) than a PbSn process, thus reducing the process window

- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 15 and 16

Table 15. SnPb eutectic process (from J-STD-020C)

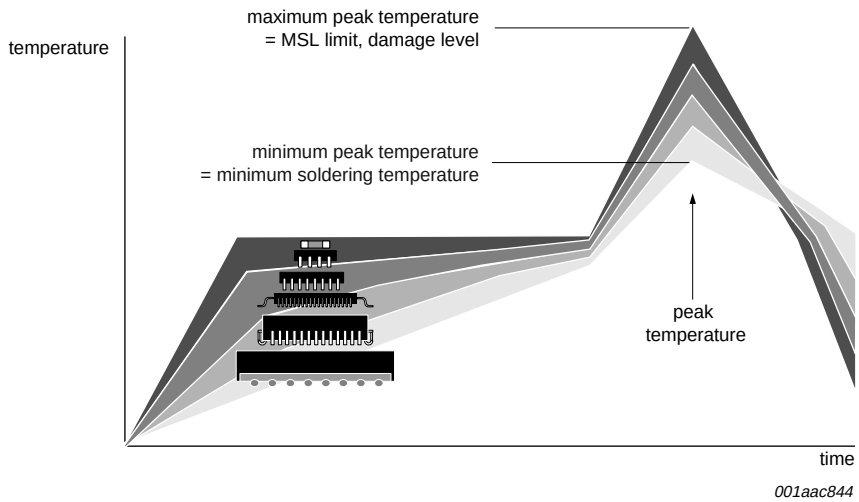
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 16. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 14.



MSL: Moisture Sensitivity Level

Fig 14. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Abbreviations

Table 17. Abbreviations

Acronym	Description
ASIC	Application Specific Integrated Circuits
ATX	Analog USB Transceiver
CMOS	Complementary Metal-Oxide Semiconductor
HBM	Human Body Model
PDA	Personal Digital Assistant
RXD	Receive Data
SE0	Single-Ended Zero
TXD	Transmit Data
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

17. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] ECN_27%_Resistor (Pull-up/pull-down Resistors ECN)

18. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ISP1110_2	20070319	Product data sheet	-	ISP1110_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 2 "Pin description": updated description for pin 6. • Section 7.1 "Modes of operation": updated Table 3 and added Table 4. • Section 7.1.1 "USB mode": updated third paragraph. • Section 7.1.2 "UART mode": updated fourth paragraph. • Table 9 "Recommended operating conditions": added T_j.			
ISP1110_1	20060323	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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continued >>

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Document identifier: ISP1110_2